

**REMARKS**

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1-20 remain pending in this application.

Reconsideration of the claims is respectfully requested.

**I. CLAIM REJECTION UNDER 35 U.S.C. § 103**

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,563,837 to *Krishna, et al.*, hereinafter “Krishna”. The Applicant respectfully traverses the rejection.

In ex parte examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. (MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)). The initial burden of establishing a prima facie basis to deny patentability to a claimed invention is always upon the Patent Office. (MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)). Only when a prima facie case of obviousness is established does the burden shift to the Applicant to produce evidence of nonobviousness. (MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)). If the Patent Office does not produce a prima facie case of unpatentability, then without more the Applicant is entitled to grant of a patent. (In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)).

A. CLAIMS 1, 4, 7, AND 14: INPUT BUFFERS EXTERNAL TO INPUT PORT

Claim 1 comprises a switch fabric that includes:

“N input buffers to receive incoming fixed-size data packets from an input port at a first data rate and to output said fixed-size data packets at a second data rate equal to at least twice said first data rate, *wherein said N input buffers are internal to said switch fabric and are external to said input port*”

Krishna does not teach or suggest this switch fabric. The Office Action has attempted to analogize this switch fabric with Krishna. Specifically, the Office Action asserts that the Claim 1 limitation of “*said N input buffers are internal to said switch fabric and are external to said input port*” is taught or suggested by Figure 1 of Krishna. However, Krishna only teaches buffers **internal** to the input port, and does teach or suggest input buffers ... external to an input port.

For the purpose of Clarity, the relevant portion of Figure 1 is reproduced below:

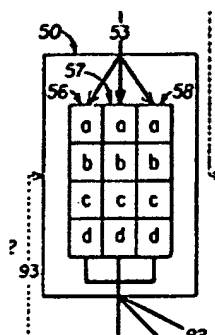


Figure 1, Element 50

In Figure 1 of Krishna “each input port 50, 51 and 52 has virtual output queues (VOQ's) 56, 57 and 58, *each containing input buffers ‘a’ through ‘d’ for storing data*” (Emphasis added, Krishna, Col. 7 ll. 5-10). Therefore, the input buffers are contained, or **internal** to, the input port of Krishna. Figure 1 illustrates this and shows that each ‘a’ through ‘d’ buffer is **internal** to input port 50.

In contrast to Krishna, Claim 1 of the pending disclosure claims that the “N input buffers are” ... “external to said input port”. Krishna does not teach or suggest that the input buffers are external to input ports. Therefore, Krishna does not teach or suggest all of the limitations of Claim 1.

Claims 4, 7, and 14 each contain limitations directed at N input buffers. These claimed N input buffers are, consistent with the N input buffers in Claim 1, external to the input port. Therefore, Claims 4, 7, and 14 are similarly patentable over Krishna.

**B. CLAIMS 1, 4, 7, AND 14: SCHEDULING CONTROLLER**

Claim 1 comprises a switch fabric that includes:

“a scheduling controller connected to the bufferless, non-blocking interconnecting network.”

Krishna does not teach or suggest this switch fabric. The Office Action has attempted to analogize the scheduling controller of this switch fabric with Krishna. Specifically, the Office Action asserts that the Claim 1 limitation of “*a scheduling controller connected to the bufferless, non-blocking interconnecting network*” is taught or suggested by Figure 1, Col. 1 ll. 22-30, and Col. 5 ll. 8-13 of Krishna. However, Krishna only teaches an arbiter that controls input and output ports. Krishna does not teach “*a scheduling controller connected to the bufferless, non-blocking interconnecting network*”.

For the purpose of Clarity, Figure 1 of Krishna is reproduced below:

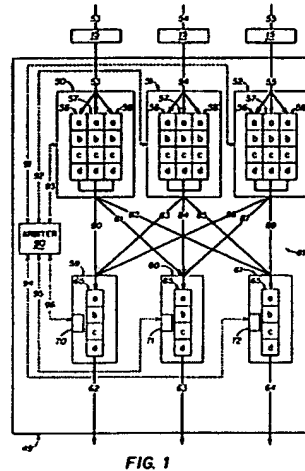


Figure 1 of Krishna illustrates that the arbiter is **not connected** to the network. The arbiter is connected only to the input and output ports. Therefore, Figure 1 does not teach or suggest “*a scheduling controller connected to the bufferless, non-blocking interconnecting network*”.

The sections from the cited paragraphs from Krishna are reproduced below:

The internal switching fabric of a network device interconnects input ports to output ports and is typically controlled by an arbiter. The arbiter typically controls the flow of data from input to output ports, using an arbitration algorithm to sequentially make matches between the ports. The switching fabric then uses the matches to transfer the data once no more matches can be made. The process of an arbiter controlling a switch fabric to interconnect input and output ports is referred to as "switching" the data. [Col. 1 ll. 22-30 of Krishna]

The above described aspects of the invention may be embodied in hardware, software or a combination of both. Moreover, the method and apparatus may be embodied within the entire network device, or may be contained primarily within the arbiter of the network device which can control the input and output ports and the switch fabric. [Col. 5 ll. 8-13 of Krishna]

It is respectfully submitted that these sections only relate to the control of the switch fabric, and do not relate to how the switch fabric is connected. Controlling the fabric is not the same as a connection to the fabric. As illustrated by Figure 3 of the original specification, there exists a connection between the scheduling controller and the bufferless crossbar. Figure 3 of the pending disclosure is reproduced herein for clarity:

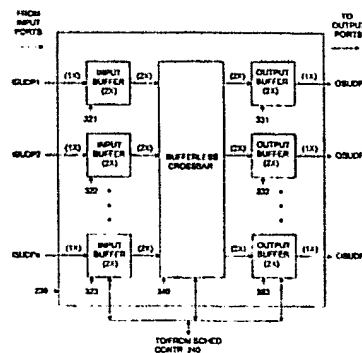


FIGURE 3

Figure 3 of the pending disclosure illustrates a “a scheduling controller connected to the bufferless, non-blocking interconnecting network”. Figure 1 of Krishna illustrates a arbiter that is not connected to a network. The cited passages of Krishna do not cure this deficiency as they do not teach or suggest how the arbiter is connected to the network. Therefore, none of the cited passages or the cited figures teach or suggest “a scheduling controller connected to the bufferless, non-blocking interconnecting network”.

Claims 4, 7, and 14 each contain limitations directed at “a scheduling controller connected to the bufferless, non-blocking interconnecting network”. Therefore, Claims 4, 7, and 14 are similarly patentable over Krishna.

**C. Claims depending from 1, 4, 7, and 14**

Claims 1-3, 5-6, 7-13, and 15-20 depend directly or indirectly from claims 1, 4, 7, and 14. Therefore, for at least the reasons set forth above, Claims 1-3, 5-6, 7-13, and 15-20 are each patentable over Krishna.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the § 103 rejections with respect to each of these claims.

**CONCLUSION**

As a result of the foregoing, the Applicant asserts that the remaining claims in the Application are in condition for allowance, and respectfully requests that this Application be passed to issue.


If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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Date: 04/24/08

  
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